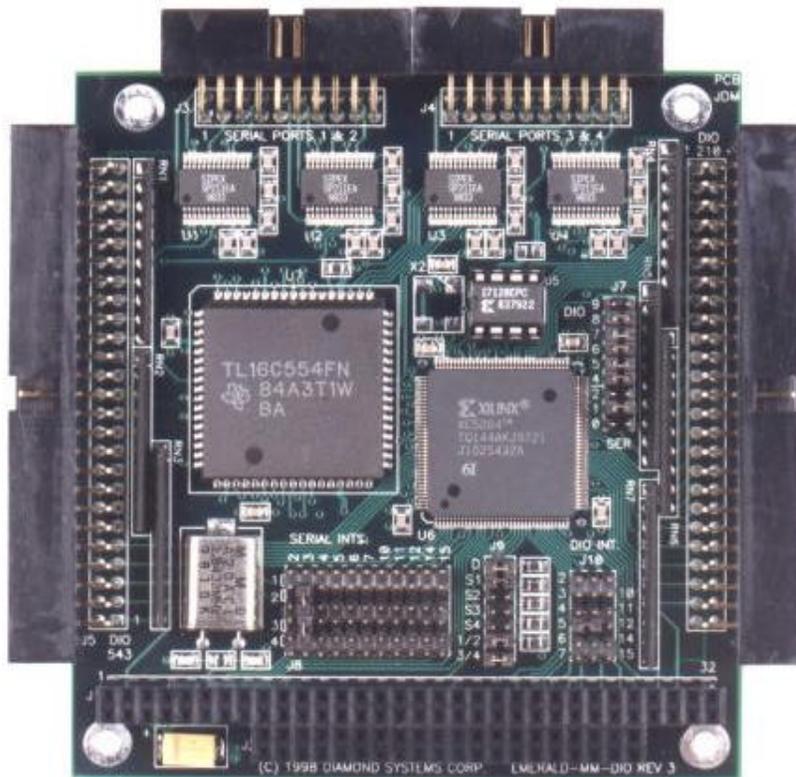


# EMERALD-MM-DIO

*Quad RS-232 + 48 Digital I/O PC/104 Module*

Board Revision V3

User Manual V2.0



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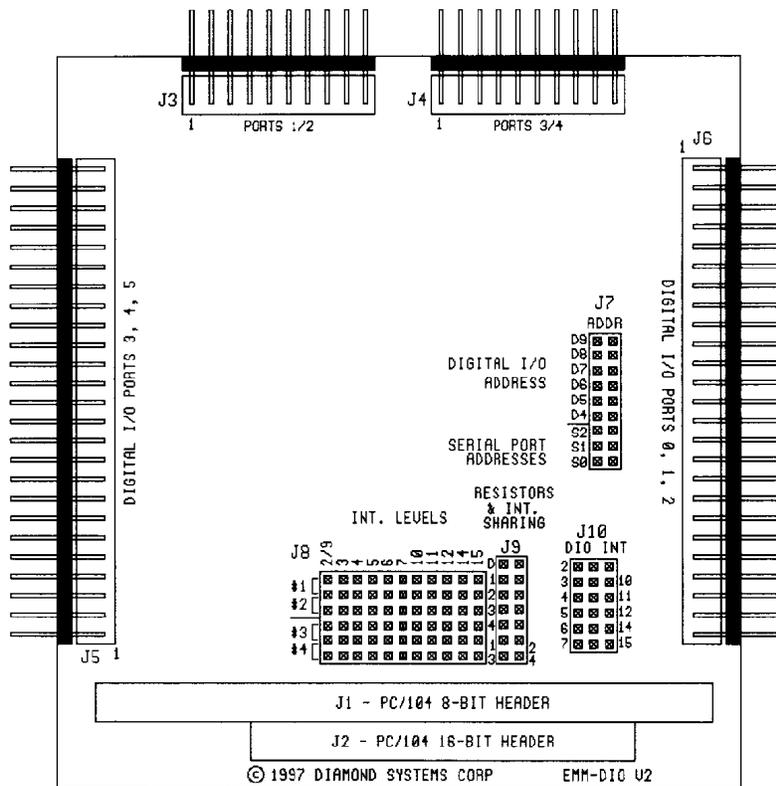
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# EMERALD-MM-DIO

Quad RS-232 + 48 Digital I/O PC/104 Module

Board Revision V3

## 1. EMERALD-MM-DIO BOARD DRAWING



DIG-ADDP010-HEN U2

- J1: PC/104 bus 8-bit connector
- J2: PC/104 bus 16-bit connector
- J3: I/O header for serial ports 1 – 2 (2x10 pins)
- J4: I/O header for serial ports 3 – 4 (2x10 pins)
- J5: I/O header for digital I/O ports 3 – 5 (2x25 pins)
- J6: I/O header for digital I/O ports 0 – 2 (2x25 pins)
- J7: Serial port and digital I/O address configuration
- J8: Serial port interrupt level selection
- J9: Interrupt pulldown and level sharing configuration
- J10: Digital I/O interrupt level selection



## 2. I/O HEADER PINOUTS

All I/O headers mate with .1" x .1" pitch dual-row ribbon cable connectors.

### 2.1 RS-232 Headers

J3			J4		
DCD 1	1	2	DSR 1	1	2
RXD 1	3	4	RTS 1	3	4
TXD 1	5	6	CTS 1	5	6
DTR 1	7	8	RI 1	7	8
GND	9	10	NC	9	10
DCD 2	11	12	DSR 2	11	12
RXD 2	13	14	RTS 2	13	14
TXD 2	15	16	CTS 2	15	16
DTR 2	17	18	RI 2	17	18
GND	19	20	NC	19	20

#### Signal Definitions:

<u>Signal Name</u>	<u>Definition</u>	<u>Direction with respect to board</u>
DCD	Data Carrier Detect	Input
DSR	Data Set Ready	Input
RXD	Receive Data	Input
RTS	Request To Send	Output
TXD	Transmit Data	Output
CTS	Clear To Send	Input
DTR	Data Terminal Ready	Output
RI	Ring Indicator	Input
GND	Ground	--

## 2.2 Digital I/O Headers

J5				J6			
Digital IO Ports 5, 4, 3				Digital I/O Ports 2, 1, 0			
Port 5 Bit 7	1	2	GND	Port 2 Bit 7	1	2	GND
Port 5 Bit 6	3	4	GND	Port 2 Bit 6	3	4	GND
Port 5 Bit 5	5	6	GND	Port 2 Bit 5	5	6	GND
Port 5 Bit 4	7	8	GND	Port 2 Bit 4	7	8	GND
Port 5 Bit 3	9	10	GND	Port 2 Bit 3	9	10	GND
Port 5 Bit 2	11	12	GND	Port 2 Bit 2	11	12	GND
Port 5 Bit 1	13	14	GND	Port 2 Bit 1	13	14	GND
Port 5 Bit 0	15	16	GND	Port 2 Bit 0	15	16	GND
Port 4 Bit 7	17	18	GND	Port 1 Bit 7	17	18	GND
Port 4 Bit 6	19	20	GND	Port 1 Bit 6	19	20	GND
Port 4 Bit 5	32	22	GND	Port 1 Bit 5	32	22	GND
Port 4 Bit 4	23	24	GND	Port 1 Bit 4	23	24	GND
Port 4 Bit 3	25	26	GND	Port 1 Bit 3	25	26	GND
Port 4 Bit 2	27	28	GND	Port 1 Bit 2	27	28	GND
Port 4 Bit 1	29	30	GND	Port 1 Bit 1	29	30	GND
Port 4 Bit 0	31	32	GND	Port 1 Bit 0	31	32	GND
Port 3 Bit 7	33	34	GND	Port 0 Bit 7	33	34	GND
Port 3 Bit 6	35	36	GND	Port 0 Bit 6	35	36	GND
Port 3 Bit 5	37	38	GND	Port 0 Bit 5	37	38	GND
Port 3 Bit 4	39	40	GND	Port 0 Bit 4	39	40	GND
Port 3 Bit 3	41	42	GND	Port 0 Bit 3	41	42	GND
Port 3 Bit 2	43	44	GND	Port 0 Bit 2	43	44	GND
Port 3 Bit 1	45	46	GND	Port 0 Bit 1	45	46	GND
Port 3 Bit 0	47	48	GND	Port 0 Bit 0	47	48	GND
+5V	49	50	GND	+5V	49	50	GND

### Signal Definitions:

<u>Signal Name</u>	<u>Definition</u>	<u>Direction with respect to board</u>
Port n Bit m	Digital I/O bit m on port n	Bidirectional Ports 0 through 2 have interrupt on state change capability
+5V	+5V power from PC/104 bus	--
GND	Ground connection on PC/104 bus	--

Note that pin 1 on J6 is at the top of the board (at the opposite end from the PC/104 bus connectors), and pin 1 on J5 is at the bottom of the board (next to the PC/104 bus connectors).

### 3. BOARD CONFIGURATION

Refer to the board drawing on page 3 for locations of the configuration items mentioned here.

#### 3.1 Address Selection

EMERALD-MM-DIO occupies 6 distinct blocks in I/O memory: One for the digital I/O, four for the serial ports, and one for the serial port interrupt status register.

##### Digital I/O Base Address

The digital I/O base address is set with jumper block J7, located on the right side of the board next to I/O header J6. The locations labeled D9 through D4 are used for the digital I/O address. These lines correspond to address lines 9 through 4. The lowest 4 address bits, numbered 3 - 0, are assumed to be 0 for the base address. The following table lists some example base address settings; many others are possible. Note that when a jumper is installed, the corresponding address line must be 0, and when a jumper is removed, the corresponding address line must be 1. Addresses below 100 Hex are reserved for the CPU, so only combinations above 100 Hex are shown here.

**Table 3.1: Jumper Block J7 - Digital I/O Base Address Configuration Examples**

<b>D9</b>	<b>D8</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>Base Address</b>
In	Out	In	In	In	In	100
In	Out	In	In	Out	In	120
In	Out	In	Out	In	In	140
In	Out	Out	In	In	In	180
Out	In	In	In	In	In	200
Out	In	In	Out	In	In	240
Out	In	Out	In	In	In	280
Out	In	Out	Out	In	In	2C0
Out	Out	In	In	In	In	300
Out	Out	In	Out	In	In	340
Out	Out	Out	In	In	In	380
Out	Out	Out	Out	In	In	3C0

### Serial Port and Interrupt Register Address Selection

These addresses are also set with jumper block J7, located at the right side of the board by I/O header J6. Eight different I/O address combinations are selectable, using the three locations marked S2, S1, S0. The address shown below for each port is the base address of that port, i.e. the lowest address of the port's I/O address block.

**Table 3.2: Jumper Block J7 - Serial Port and Interrupt Status Register Addresses**

No.	S2	S1	S0	Port 1	Port 2	Port 3	Port 4	Interrupt Status
0	In	In	In	3F8	2F8	3E8	2E8	220
1	In	In	Out	3E8	2E8	3A8	2A8	220
2	In	Out	In	380	388	288	230	224
3	In	Out	Out	240	248	260	268	224
4	Out	In	In	100	108	110	118	240
5	Out	In	Out	120	128	130	138	244
6	Out	Out	In	140	148	150	158	248
7	Out	Out	Out	160	168	170	178	24C

### 3.2 Serial Port Interrupt Level Selection

The serial port interrupt levels are selected with jumper block J8 at the bottom of the board. The interrupt level for each port is selected by installing a jumper across two rows underneath the desired level number as follows:

Port 1	Rows 1 and 2
Port 2	Rows 2 and 3
Port 3	Rows 4 and 5
Port 4	Rows 5 and 6

Note that ports 1 and 2 share row 2, and ports 3 and 4 share row 5. As long as ports 1 and 2 do not share the same interrupt level, there is no conflict, and the same applies for ports 3 and 4.

If sharing is to be enabled for ports 1 and 2, then install a jumper under the desired interrupt level for either port 1 or port 2, and then install another jumper across the pins marked 1 and 2 in jumper block J9, located to the right of J8. These pins are on the row second from the bottom.

Similarly, if sharing is to be enabled for ports 3 and 4, then install a jumper under the desired interrupt level for either port 3 or port 4, and then install another jumper across the pins marked 3 and 4 in jumper block J9, located to the right of J8. These pins are on the bottom row of J9.

### 3.3 Digital Interrupt Level Selection

The digital input interrupt level is selected by installing a jumper next to the desired level number on jumper block J10. The jumper is installed so that one of the pins it fits over is in the middle column, and the second pin is on one of the outer columns, depending on the level selected. For example, to select level 3, install a jumper next to the number 3 so that it fits over the left and middle columns. To select level 14, install a jumper next to the number 14 so that it fits over the middle and right columns.

### 3.4 Interrupt Pulldown Resistor Enabling

On the PC/104 bus, interrupt lines that are to be shared require a 1K $\Omega$  pulldown resistor to pull the line low when no device is driving it active to request interrupt service. Jumper block J9 is used to enable the pulldown resistors. Install a jumper across both pins next to the device for which you want to enable the resistor: 1 - 4 selects the same-numbered serial port, and D selects the digital interrupt. To disable the pulldown resistor, pull out the jumper or install it over only one pin.

Note that if you have interrupt sharing enabled, only one jumper should be installed for all ports sharing the same level. Otherwise you will have too low an impedance on the line, and the board will not be able to drive the signal to a logic 1 level to request interrupt service.

For example, if you are sharing interrupts on ports 1 and 2, but ports 3 and 4 are using different interrupt levels, then install jumpers in J9 next to positions 1, 3, and 4 or positions 2, 3, and 4. Do not install a jumper in both the 1 and 2 positions.

If the digital I/O is sharing an interrupt level with one of the serial ports, then the same applies: do not install a jumper in both the D position and the serial port number position.

### 3.5 Default Settings

The default settings for EMERALD-MM-DIO are as follows:

I/O address	200 Hex, see Table 3.1 above
Serial ports	Selection 5 in Table 3.2 above
Serial port interrupts	All 4 ports sharing level 3
Interrupt pulldown resistors	Enabled on serial interrupts and digital interrupt; remaining serial port jumpers are present over only one pin

## 4. DIGITAL I/O OPERATION

The digital I/O circuitry occupies 16 bytes, with the base address selected with jumper block J7 as described on page 7. Not all addresses are used; however all are reserved by the board.

All internal registers reset to 0 asynchronously upon power up or system reset.

The base address is set with jumpers 9 – 4 on jumper block

### 4.1 Digital I/O Address Map

<b>Base +</b>	<b>Write Function</b>	<b>Read Function</b>
0	Port 0 DIO	Port 0 DIO
1	Port 1 DIO	Port 1 DIO
2	Port 2 DIO	Port 2 DIO
3	Port 3 DIO	Port 3 DIO
4	Port 4 DIO	Port 4 DIO
5	Port 5 DIO	Port 5 DIO
6	N/A	Digital I/O interrupt status register
7	Page / Lock register (3 pages)	N/A
8	Maps to register 0 of current page	
9	Maps to register 1 of current page	
10	Maps to register 2 of current page	
11	N/A	N/A
12	N/A	N/A
13	N/A	N/A
14	N/A	N/A
15	N/A	N/A

## 4.2 Page Registers

The Page/Lock register at address base + 7 contains two bits which select the current page accessed by locations 8 - 10. Four pages are addressable with these two bits. Page 0 registers are not used; only pages 1 through 3 are defined. Each page contains three registers as described below. These registers are used to control the behavior of the edge detection circuitry which exists for the 24 I/O bits in DIO registers 0 through 2.

### Page 1 registers:

<b>Offset</b>	<b>Write Function</b>	<b>Read Function</b>
0	Pol_0	Pol_0
1	Pol_1	Pol_1
2	Pol_2	Pol_2

These three 8 bit read/write registers are used to indicate the polarity of edges detected by the edge detection circuit. A 0 in a bit position enables falling edge detection on the corresponding I/O bit, and a 1 enables rising edge detection. Pol\_0 corresponds to DIO register 0, Pol\_1 to DIO register 1, and Pol\_2 to DIO register 2.

### Page 2 registers:

<b>Offset</b>	<b>Write Function</b>	<b>Read Function</b>
0	Enab_0	Enab_0
1	Enab_1	Enab_1
2	Enab_2	Enab_2

These three 8-bit read/write registers are used to individually enable or disable edge detection on each bit in the corresponding I/O registers. A 0 in a bit position disables edge detection on the corresponding bit, and a 1 enables edge detection for that bit. Enab\_0 corresponds to DIO register 0, Enab\_1 to DIO register 1, and Enab\_2 to DIO register 2.

### Page 3 registers:

<b>Offset</b>	<b>Write Function</b>	<b>Read Function</b>
0	Clear edge detect bits for DIO 0	Int_ID_0
1	Clear edge detect bits for DIO 1	Int_ID_1
2	Clear edge detect bits for DIO 2	Int_ID_2

Reading from these three locations returns the status of the edge detection circuit for each bit. A 1 in a bit position indicates that that bit experienced the edge indicated by the corresponding bit in the corresponding Pol register AND that bit is enabled with a 1 in the corresponding bit in the corresponding Enab register.

Writing to any of these addresses clears all the edge detect bits for the corresponding group of 8 I/O lines. Register 0 corresponds to DIO register 0, etc.

## 5. DIGITAL I/O REGISTER DESCRIPTIONS

These are the on-board registers decoded with DIOSW[9-4].

### Base + 0 to 5    Read/Write    Digital I/O Data

Bit No.	7	6	5	4	3	2	1	0
Name	D[n][7]	D[n][6]	D[n][5]	D[n][4]	D[n][3]	D[n][2]	D[n][1]	D[n][0]

#### Definitions:

D[n][7-0]    Digital I/O data; n is the port number 0 - 5, corresponding to addresses base + 0 through base + 5.

When reading from a port, the value read is the opposite polarity from the state of the pin.

When a 0 is written to the port, the port's output pin is tristated, and an external 10KΩ resistor pulls the pin to a logic 1 level. When a 1 is written to the port, the port's output pin is driven low.

### Base + 6    Read    Interrupt Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	INT2	INT1	INT0

#### Definitions:

X    Not used

INT2-0    Interrupt pending on port 2-0:

0 = no interrupt pending, 1 = interrupt pending

### Base + 7    Write    Page / Lock Register

Bit No.	7	6	5	4	3	2	1	0
Name	P1	P0	Lock5	Lock4	Lock3	Lock2	Lock1	Lock0

#### Definitions:

P1-0    Page number. Defines which page of registers is accessed at base + 8 through base + 10.

P1	P0	Page
0	0	Not used
0	1	Polarity registers
1	0	Enable registers
1	1	Interrupt ID registers / Clear Interrupts

Lock5-0    Controls write access to ports 5-0. A 1 in a bit position prohibits data being written to the associated port. A 0 enables writing data to that port.

## Page Registers:

### Page 1:

#### Base + 8 to 10 Read/Write Edge Polarity POL[0-2]

Bit No.	7	6	5	4	3	2	1	0
Name	Pol[n][7]	Pol[n][6]	Pol[n][5]	Pol[n][4]	Pol[n][3]	Pol[n][2]	Pol[n][1]	Pol[n][0]

#### Definitions:

Pol[n][m] Polarity for edge detection circuit on port n, bit m. n = 0 to 2, m = 0 to 7. If the bit is a 0, negative edges are detected by the edge detection circuit, and if the bit is a 1, positive edges are detected. Edges are only detected if the associated Enable bit is a 1 (see page 2 registers below).

### Page 2:

#### Base + 8 to 10 Read/Write Edge Detect Enable ENAB[0-2]

Bit No.	7	6	5	4	3	2	1	0
Name	Enab[n][7]	Enab[n][6]	Enab[n][5]	Enab[n][4]	Enab[n][3]	Enab[n][2]	Enab[n][1]	Enab[n][0]

#### Definitions:

Enab[n][m] Enables edge detection on port n, bit m. n = 0 to 2, m = 0 to 7. If the bit is a 0, edge detection is disabled for that input line, and if the bit is a 1, edge detection is enabled. The polarity of the edge that is detected is controlled with the polarity registers in page 0 (see page 1 registers above).

### Page 3:

#### Base + 8 to 10 Write Edge Detection Clear CLEAR[0-2]

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	X

#### Definitions:

X Not used

Writing to the page 3 register at base + 8 clears all edge detect circuits for port 0, writing to base + 9 clears port 1, and writing to base + 10 clears port 2. The value written does not matter.

#### Base + 8 to 10 Read Edge Detection Status INT\_ID[0-2]

Bit No.	7	6	5	4	3	2	1	0
Name	ID[n][7]	ID[n][6]	ID[n][5]	ID[n][4]	ID[n][3]	ID[n][2]	ID[n][1]	ID[n][0]

#### Definitions:

ID[n][7-0] Edge detection status for port n, bit 7-0. A 1 indicates that the programmed edge was detected since that last clear, and a 0 indicates that no edge was detected.

## 6. SPECIFICATIONS

### Serial Ports

No. of serial ports	4, RS-232
Maximum baud rate	115kbps
Communications parameters	5, 6, 7, or 8 data bits; Even, odd, or no parity
Short circuit protection	All outputs protected against continuous short circuit
Input impedance	3K $\Omega$ min
Input voltage swing	$\pm$ 30V max
Output voltage swing	$\pm$ 5V min, $\pm$ 7V typical

### Digital I/O

No. of lines	48
Direction	Programmable bit by bit
Edge detection	Enable and polarity both programmable bit by bit
Input voltage:	
Logic 0	0.0V min, 0.8V max, $\pm$ 10 $\mu$ A max
Logic 1	2.0V min, 5.0V max, $\pm$ 10 $\mu$ A max
Output voltage:	
Logic 0	0.0V min, 0.4V max, 8mA max output current
Logic 1	3.86V min, 5.0V max, 0.3mA max output current

### General

I/O headers:	(All I/O headers mate with standard ribbon cable (IDC) connectors)
Serial ports	2 20-position (2x10) headers
Digital I/O	2 50-pin (2x25) headers
Dimensions	3.55" x 3.775" LxW (PC/104 standard)
Power supply	+5VDC $\pm$ 5%
Current consumption	100mA typical, all outputs unloaded
Operating temperature	-40 to +85 $^{\circ}$ C
Operating humidity	5% to 95% noncondensing
PC/104 bus	8 bit and 16-bit bus headers are installed (16-bit header is used for interrupt levels only)